ABSTRACT OF THE DISCLOSURE

A semiconductor memory device, that reduces load capacitance of write-only bit lines, may include: a first bit cell array block, in which bit cells thereof are defined by intersections of first bit lines and first word lines, the first bit lines being arranged as pairs of first signal lines and second signal lines, respectively; a second bit cell array block, in which bit cells thereof are defined by intersections of second bit lines and second word lines, the second bit lines being arranged as pairs of third signal lines and the second signal lines; respectively; a block division circuit operable to generate and output block division control signals; and a write bit line divider circuit operable to either open-circuit or connect together the first signal lines and the third signal lines, respectively, according to the block division control signals.